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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/511,079	10/12/2004	Ken Ozawa	075834.00464	6553

33448 7590 11/08/2007

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EXAMINER	
ROSASCO, STEPHEN D	
ART UNIT	**PAPER NUMBER**
1795	

MAIL DATE	DELIVERY MODE
11/08/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/511,079	OZAWA, KEN	
	Examiner	Art Unit	
	Stephen Rosasco	1795	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 April 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12 October 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *10/12/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Detailed Action

Claim 1 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Claim 1 paragraph 3 is unclear "...that allows...on said wafer matches".

The Drawings are objected to: Fig. 8, box S3, should read –Dimensions ON-.

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-4 are rejected under 35 U.S.C. 102(e) as being anticipated by Chen et al. (6,420,077) or Ohnuma (6,928,636).

Chen et al. address claims 1-4 (see claims) including a contact hole model-based optical proximity correction method, comprising the steps of: providing a photomask; forming a plurality of rectangular test patterns on a photomask with each test pattern having a plurality of contact holes having different line widths but identical distance of separation on a photomask, wherein line width is the side of each contact hole and the distance of separation is the distance from a point along

the side of the contact hole to the same position of a neighboring contact hole; performing a photo-exposure of a photoresist layer on a silicon chip using a photomask with the test patterns thereon and developing the photoresist layer to obtain a plurality of test patterns having different line widths but identical distance of separation on the silicon chip; measuring the line widths of the test patterns on the silicon chip; comparing the line widths of the test patterns on the silicon chip with the line widths of the test patterns on the photomask; and establishing a contact hole model for selecting suitable line widths from the panel of test patterns so that contact holes can be precisely reproduced in an actual photolithographic pattern transfer operation.

And (col. 4, line 63+) - As shown in FIG. 3A, the square contact hole 302 in test pattern 300 has a line width 204. Distance of separation or pitch from one contact hole 302 to its neighboring contact hole is labeled 306. For example, line width 204 of the square contact hole 302 in test pattern 300 is 0.8 .mu.m and distance of separation between neighboring contact holes is 0.8 .mu.m. Similarly, line width of contact hole 312 in test pattern 310 is 0.4 .mu.m and distance of separation between neighboring contact holes 312 is 0.8 .mu.m. Finally, line width of contact hole 316 in test pattern 314 is 0.2 .mu.m and distance of separation between neighboring contact holes 316 is 0.8 .mu.m. The test patterns 300, 310 and 314 have contact holes of different line widths but identical distance of separation between neighboring holes. The ratio between line width and distance of separation

between neighboring lines called pitch ratio is an important design parameter. For example in FIG. 3, the test pattern 300 has a pitch ratio of 0.8:0.8, that is, 1:1. On the other hand, the test pattern 310 has a pitch ratio of 0.4:0.8, that is, 1:2. Similarly, the test pattern 314 has a pitch ratio of 0.2:0.8, that is, 1:4. In other words, each test pattern in FIG. 3 is established using a different pitch ratio of the contact holes.

Ohnuma teach a rule-based OPC evaluating method comprising the steps of: obtaining correction data by correcting design data about an initial mask pattern through rule-based OPC; forming said initial mask pattern into an initial mask based on said correction data; forming gate patterns into an initial wafer using said initial mask; obtaining measured data about said initial gate patterns by measuring lengths of said initial gate patterns formed on said initial wafer; creating a simulation-based OPC model through execution of process calibration based both on test pattern design data about a test-use mask for process calibration purposes, and on measured data about gate patterns of a test-use wafer fabricated using said test-use mask; obtaining simulation data by simulating said design data about said initial mask pattern using said simulation-based OPC model; evaluating said rule-based OPC by comparing said measured data about said initial gate patterns with said simulation data; and establishing a correction grid constituting a minimum increment in which to correct said mask pattern, wherein said design data about said initial mask pattern are corrected based on said correction grid.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Toyama et al. (6,821,683).

The claimed invention is directed to a method for correcting a photo mask, which allows the difference between a test mask and a corrected mask with respect to an error of line width depending on coarse/dense pattern to be decreased when the photo masks are corrected by optical proximity effect correction. The method including producing a test mask which acts as a mask for extracting process model for applying an optical proximity effect correction method (s1); transferring and measuring the dimensions of the transferred pattern using the test mask (s2 and s3); obtaining a function model (referred to as process model) of which a simulated result of the transferred pattern of a mask pattern of the photo mask using a function model matches the measured result (s4); obtaining a mask pattern of which a transferred pattern matches a designed pattern using said process model and creating mask data in accordance with the obtained mask pattern (s5); producing a corrected mask in accordance with the created mask data (s5); and setting an exposing condition where an OPE characteristic becomes flat with respect of wide and narrow pitches by adjusting at least one of a numerical aperture (NA) and a coherence factor (sigma) of an exposing device when the corrected mask is transferred.

Toyama et al. (see claims) teach a method for correcting design pattern data in fabrication of a semiconductor in which figure patterns are formed on a semiconductor

wafer using design pattern data designed for a semiconductor circuit and transferring the figure patterns of a photomask corresponding to the design pattern data from the photomask to the semiconductor wafer by exposure, said method comprising; (A) extracting a data/wafer difference by: obtaining said figure patterns of the semiconductor wafer corresponding to a particular pattern data made up of (1) test pattern data or (2) test pattern data combined with said design pattern data by simulation by assuming that the photomask is fabricated from said design pattern data with fidelity; and extracting a difference between said particular pattern data and said figure patterns of the semiconductor wafer corresponding to the result of the simulation; (B) extracting a data/mask difference by: forming said figure patterns corresponding to said particular pattern data on the photomask by use of said particular pattern data according to a specified method of fabricating a photomask; and measuring said figure patterns formed on the photomask, thereby extracting a difference between said particular pattern data and said figure patterns of the photomask; (C) deriving an amount of correction to transform the shape of said particular pattern data on the basis of said data/mask difference and said data/wafer difference in such a manner that the difference between said particular pattern data and the corresponding figure patterns of the semiconductor wafer becomes smaller; and (D) correcting the shape of the design pattern data by use of the amount of correction to generate corrected design pattern data.

The teachings of Toyama et al. differ from those of the applicant in that the applicant teaches specific

However, it would have been obvious that in a range of the pattern pitch which is wide enough the OPE characteristic would become flat. The OPE is a function of the

spacing of the pattern features and when the spacing is large enough the effect is minimized. And that the exposure conditions including NA and coherence factor would also affect the OPE.

Therefore, the examiner holds that it would have been obvious to one having ordinary skill in the art to take the teachings of Toyama et al. and combine them with a general knowledge of the prior art in order to make the claimed invention because it would have been obvious that in a range of the pattern pitch which is wide enough the OPE characteristic would become flat.

Conclusion

Any inquiry concerning this communication or earlier communications from the Examiner should be directed to Stephen Rosasco whose telephone number is (571) 272-1389. The Examiner can normally be reached Monday-Friday, from 8:00 AM to 4:30 PM. The Examiner's supervisor, Mark Huff, can be reached on (571) 272-1385. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

S. Rosasco
Primary Examiner
Art Unit 1756

S.Rosasco
11/05/07